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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/817,113	04/01/2004	Buo-Chin Hsu	D&F-041	2814
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BEVER HOFFMAN & HARMS, LLP TRI-VALLEY OFFICE 1432 CONCANNON BLVD., BLDG. G LIVERMORE, CA 94550			MONDT, JOHANNES P	
			ART UNIT	PAPER NUMBER
			3663	

DATE MAILED: 11/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

Application No.

10/817,113

Applicant(s)

HSU ET AL.

Examiner

Johannes P. Mondt

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 02 September 2005.  
2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.  
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-14 is/are pending in the application.  
4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.  
5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.  
6) ☒ Claim(s) 1-14 is/are rejected.  
7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.  
8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.  
10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☒ All b) ☐ Some \* c) ☐ None of:  
1. ☒ Certified copies of the priority documents have been received.  
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)  
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)  
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_.  
4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date \_\_\_\_\_.  
5) ☐ Notice of Informal Patent Application (PTO-152)  
6) ☐ Other: \_\_\_\_\_.

## DETAILED ACTION

### *Response to Amendment*

Response filed 9/2/2005 forms the basis of this office action. Comments on Remarks in said Response are included below under "Response to Arguments".

### ***Claim Rejections - 35 USC § 102***

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. ***Claim 1, 5-8 and 11-14*** are rejected under 35 U.S.C. 102(b) as being anticipated by Shields (WO 02/11211 A2). Shields teaches (Figures 3-5 (absorption of light in quantum dot), 7 (for structural details), 18 for specific embodiment of the layer stack comprising the quantum dot comprising semiconductor layer, the conductive layer and the insulating layer; and Figure 20 for use in an array):

an infrared photodetector (Ge absorbs light in the infrared portion of the spectrum), comprising:

a conducting layer 31 (page 21, final par.);

a semiconductor layer 47/49 comprising at least one layer 45 of quantum structure for confining a carrier in a barrier (discussion Figure 18, pages 29-30):  
the barrier being the quantum dot material);

an insulating layer (any of layers 37, 39 or 41) (discussion Figure 18, pages 29-30) formed between said conducting layer and said semiconductor layer;

a voltage source (page 17, final par.) connected to said conducting layer and said semiconductor layer for providing a bias voltage to generate a quantum tunneling effect, such that said carrier penetrates through said insulating layer to form a current (page 20, pars. 4 and 5);

wherein, when irradiated by infrared light, said carrier in said barrier absorbs the energy of said infrared light to jump out of said barrier (page 20, pars. 4 and 5) and is collected by an electrode 53 (Figure 7 and discussion thereof on pages 22-23) to form a photocurrent (loc.cit.). In conclusion, Shields anticipates claim 1.

*On claim 5:* said conducting layer is a reticular layer 103 when part of a segmented photodetector (cf. Fig. 20 and discussion thereof on page 31).

*On claim 6:* said semiconductor layer 47/49 is an p-type semiconductor (Figure 18 and discussion thereof on pages 29-30) (47 is both p-type and n-type, being undoped, while 49 is p-type through doping).

*On claim 7:* said quantum structure is a quantum dot (Figure 18, discussion thereof on pages 29-30).

*On claim 8:* said semiconductor layer comprises a Si substrate 33 (Figure 7 and discussion on pages 22-23) and plural layers of quantum structures for

instance 39 and 45 (Figure 18 and pages 29-30) formed on said Si substrate (Figure 18).

*On claim 11:* said insulating layer 37 has a thickness of 8nm thus meeting the claim limitation; said insulating layer 39 has a thickness of 5 nm thus meeting the claim; and said insulating layer 41 has a thickness of 8 nm thus meeting the claim limitation (Figure 18 and discussion thereof on pages 29-30).

*On claim 12:* the further limitation of this claim fails to further distinguish the claimed infrared photodetector over the prior art but instead only further limits its method of making.

*On claim 13:* Shields teaches (Figures 3-5 (absorption of light in quantum dot), 7 (for structural details), 18 for specific embodiment of the layer stack comprising the quantum dot comprising semiconductor layer, the conductive layer and the insulating layer; and Figure 20 for use in an array):  
an infrared photodetector (Ge absorbs light in the infrared portion of the spectrum), comprising:

a conducting layer 31 (Figures 7 and 18: pages 22-23 and 29-30);

a p-type semiconductor layer 47/49 (Figure 18) comprising at least one layer 45 of quantum structure for confining a carrier in a barrier (Figure 18 and pages 29-30: the barrier being the quantum dot material);

an insulating layer (any of layers 37, 39 or 41) (pages 29-30) formed between said conducting layer and said semiconductor layer (Figure 7 and pages 22-23);

a voltage source (pages 17-18) with a positive electrode connected to said conducting layer with a negative electrode connected to said p-type semiconductor layer (loc.cit.) for providing a bias voltage to generate a quantum tunneling effect, such that said carrier penetrates through said insulating layer to form a current (loc.cit.);

wherein, when irradiated by infrared light, said carrier in said barrier absorbs the energy of said infrared light to jump out of said barrier (pages 20-21) and is collected by an electrode 53 (Figure 7 and pages 22-23) to form a photocurrent (loc.cit.). In conclusion, Shields anticipates claim 13.

*On claim 14:* Shields teaches (Figures 3A, (absorption of light in quantum dot and consequent excitation and tunneling of electron to collector), 7 (for structural details), 15 for specific embodiment of the layer stack comprising the quantum dot comprising semiconductor layer, the conductive layer and the insulating layer):

an infrared photodetector (Ge absorbs light in the infrared portion of the spectrum), comprising:

a conducting layer 49(Figure 15 and pages 27-28);

an n-type semiconductor layer 45 (Figure 15; N.B.: undoped InAs inherently has n-type conductivity: see O. Madelung, "Semiconductors – Basic Data", p. 154 on electron mobility) comprising at least one layer of a quantum structure for confining a carrier in a barrier (quantum dots in 45);

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an insulating layer 47 (InGaAs: encapsulation: pages 25-26) formed between said conducting layer and said semiconductor layer (Figure 7 and pages 20-21);

a voltage source with a negative electrode connected to said conducting layer and with a positive electrode connected to said n-type semiconductor layer for providing a bias voltage to generate a quantum tunneling effect, such that said carrier penetrates through said insulating layer to form a current (discussion of Figure 3A on pages 19-20);

wherein, when irradiated by infrared light, said carrier in said barrier absorbs the energy of said infrared light to jump out of said barrier and is collected by an electrode connected to the conducting layer (collector) (Figure 7 and pages 22-23), to form a photocurrent (loc.cit.). In conclusion, Shields anticipates claim 14.

### ***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. **Claim 2** is rejected under 35 U.S.C. 103(a) as being unpatentable over Shields (WO 02/11211 A2) in view of Thomas et al (JP2002198503A). As detailed above, Shields anticipates claim 1. Shields also teaches said conducting layer 31 to be a doped silicon layer (Figure 18 and col. 17, l. 63-65), but does not necessarily teach said doped

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silicon to be doped polysilicon. However, (a) polysilicon is well known in the art as emitter material, as witnessed by Thomas et al ("Solution", first sentence, in English abstract); while (b) Applicant is reminded that it has been held that mere selection of known materials generally understood to be suitable to make a device, the selection of the particular material being on the basis of suitability for the intended use, would be entirely obvious. In re Leshin 125 USPQ 416. *Motivation* to select poly-silicon rather than amorphous or monocrystalline silicon at least stems from the lower thermal budget needed for its deposition.

5. **Claims 3-4** are rejected under 35 U.S.C. 103(a) as being unpatentable over Shields (WO 02/11211 A2) in view of Akama (5,679,960). As detailed above, Shields anticipates claim 1. *Shields does not necessarily teach* said conductive layer to be a transparent electrode (claim 3), nor said transparent electrode to be made of indium-tin-oxide (ITO). . *However*, (a) in the art of emitter electrodes the use of ITO electrodes for their transparency as emitter electrodes in optoelectronic devices has long been known to be *obvious* for the specific advantage that their transparency admits a reduction of the loss of light, as witnessed for example by Akama (col. 28, l. 41-52), while (b) Applicant is reminded in this regard that it has been held that mere selection of known materials generally understood to be suitable to make a device, the selection of the particular material being on the basis of suitability for the intended use, would be entirely obvious. In re Leshin 125 USPQ 416. Motivation to include the teaching by Akama at least derives from the need to minimize loss of optical input in the photodetector art.



6. **Claim 9** is rejected under 35 U.S.C. 103(a) as being unpatentable over Shields (WO 02/11211 A2) in view of Kibbel et al (US 2002/0112755 A1). As detailed above, Shields anticipates claim 1. Shields does not necessarily teach the further limitation defined by claim 9. However, Shields does teach that the quantum dots can be made by the Stranski-Krastanow method (col. 6, l. 40-43) in which quantum dots are grown in a self-assembled way on a wetting layer. Furthermore, it is at least in accordance with said Stranski-Krastanov method to grow the Ge dots of Shields in a self-assembled way on a Ge wetting layer, as witnessed by Kibbel et al (see paragraph [0020]). Motivation to include the teaching by Kibbel et al at least derives from the recommendation in Shields itself when coupled with the relative simplicity of using a wetting layer of identical constitution.

7. **Claim 10** is rejected under 35 U.S.C. 103(a) as being unpatentable over Shields (WO 02/11211 A2) in view of Berger et al (US 2003/0049894 A1). As detailed above, Shields anticipates claim 1. Shields does not necessarily teach the further limitation of claim 10. *However, it would have been obvious to include said further limitation in view of Berger et al*, who, in the art of tunneling barriers for devices based on silicon technology (title, abstract and par. [0003]) (hence closely related to the problem of the selection of tunnel barrier material) that SiO<sub>2</sub> is preferred as tunnel insulating layer material as it is compatible with silicon technology. Because the infrared photodetector of Figure 18 is indeed based on Si technology (col. 17, l. 58-61) *motivation* exists to make the tunnel insulating layer to be a silicon oxide layer.

### ***Response to Arguments***

Applicant's arguments filed 9/2/2005 have been fully considered but they are not persuasive. In particular, with regard to the comments in traverse of the rejections under 35 U.S.C. 102(b) over Shields et al, - see pages 2-3, on the issue of the claimed insulating layer: in spite of embodiments showing a quantum well structure in the semiconductor layer of Applicant's specification, no such quantum well layer was claimed, nor is one claimed now. That tunnel barrier layers are incomplete insulators, in that they allow under certain circumstances tunneling of particular charge carriers, does not detract from their insulating nature: in fact, their insulating nature is a sine qua non for their required function as tunnel barriers. Therefore, short of an amendment wherein the independence of the insulating layer of Applicant is claimed it appears that the prior art in the form of Shields et al does anticipate the insulating layer as claimed. Also in the application as claimed (claim 1) carriers must be able to tunnel through any insulating layer of the prior art that meets the claim limitation, because of lines 7-9. Therefore, the arguments of Applicant on the issue of the claimed insulating layer are found not to be persuasive. Parenthetically, if, *arguendo*, an insulating layer were claimed to be separate from any quantum well structure, which is not the case thus far, then layer 35, being both semiconducting and insulating by virtue of its undoped character (see page 28, line 26), would meet the claim limitation on insulating layer as well.

Furthermore, with regard to the arguments in traverse on the issue of the semiconductor layer (pages 3-4 of Remarks), the italic bold portion as taken from the

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specification, [0030], does not require the semiconductor layer to have a quantum well, but only requires said semiconductor layer to have at least one layer of quantum well OR quantum dot, which is met because the quantum dot layer 45 belongs to the semiconductor layer 47/49, and thus the specific nature of the underlying quantum well structure is not part of the subject matter already claimed at the stage when the insulating layer is introduced in the claim language. Neither is there a limitation anywhere else in the claim on having, in addition to and included in the claimed semiconductor layer, a quantum well. That, according to Applicant on page 4 of Remarks, it is recited that "a semiconductor layer comprising at least one layer of quantum structure for confining a carrier in a barrier, an insulating layer.." does not invalidate the insulating layer as meeting the claim limitation, because said insulating layer in the prior art is separate from the quantum dots that form the barriers.

Finally, the allegedly novel feature of metal-insulator-semiconductor rather than conventional metal-semiconductor-metal structure, viz. Remarks, page 4, finds no representation in the present claim language.

Therefore, the rejections made in the office action mailed 6/3/05 must regrettably be made to stand.

### ***Conclusion***

**THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within

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TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Johannes P. Mondt whose telephone number is 571-272-1919. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack W. Keith can be reached on 571-272-6878. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JPM  
November 17, 2005

  
**JACK KEITH**  
**SUPERVISORY PATENT EXAMINER**